EE 101: Electrical & Electronics Workshop

Lecture Schedule		**Course Type, Semester**	Fundamental Engineering, Second
Credit Hours	Zero + One	**Pre-requisite**	
Instructor		**Contact**	arsalanarahim@uet.edu.pk engr.mohammadijaz@gmail.com
Office	Room # 214, First Floor, Department of Electrical Engineering	**Office Hours**	Tuesday and Thursday 9:00 pm – 12:00 pm
Lab Instructors	Mr. Arsalan A Rahim Mr. Muhammad Ijaz	**Lab Schedule**	See Time Table
Course Description	This lab course is intended to provide students with the first hands on usage of tools, skills and software expertise for design, placement and soldering on Vero-board and PCB. This lab will be the foundation lab for other lab courses in future and their project visualization into hardware form. Students will have a deep understanding of different tools and software's required for PCB designing, etching, drilling and soldering with usage of different semiconductor devices from LED Bars, Seven Segment displays, Dot Matrix Display, Relays. The lab course will also get student informed from different wiring schemes used in house hold with introduction of different actuators, sensors as well.		
Grading Policy vis-à-vis CLO Mapping	• Lab RUBRIC (Individual marks): 25% CLO-1 • Vero Board Projects: (Group) 20% CLO-2 • PCB Projects: (Group) 25% CLO-3 • Lab Project: (Group) 30% CLO-4		
	•		

Laboratory Plan

Measurable Learning Outcomes	CLOs	Description	Domain	Taxonomy Level	PLO
	CLO1	Demonstrate the basic tools needed for electrical and electronics workshop	Psychom-otor	3	PLO5, High
	CLO2	Construct a Vero-board based circuit for different electrical & semiconductor circuits	Psychom-otor	4	PLO3, High
	CLO3	Develop and design of printed circuit boards for electrical & semiconductor circuits	Psychom-otor	4	PLO5, High
	CLO4	Demonstrate the working of different electrical actuators, transducers and wiring schemes.	Psychom-otor	3	PLO9, Low

Lab Plan

Laboratories	Topics	CLOs
1*	Introduction to Basic lab tools & equipment with demonstration	CLO1
1*	How to use a Vero Board for simple Single Digit Seven Segment Display with Soldering	CLO2
1	Usage of 4x Seven Segments with BCD IC on Vero Board	CLO2
1	Soldering of Bar Display on Vero board with Dip Switches	CLO2
1*	Soldering of Dot Matrix on Vero Board with Dip Switches	CLO2
1	Introduction to PCB Design Tool Altium and design of single layer PCB	CLO3
1	Introduction to Toner Transfer Method for PCB with Etching and Drilling	CLO3
1	Seven Segment & Dot Matrix PCB Single Layer (with vias)	CLO3
1*	Introduction to two Layer PCB design and Fabrication with SMD Component (TO-92, SOIC, TSSOP) placement	CLO3
1	Introduction to Negative / Positive Photo resist Method for PCB	CLO3
1	Introduction to De-soldering & usage of Hot Air Gun for SMD Components	CLO1
1	Introduction to Relays (5V & 12V) with PCB footprint, usage and Driver	CLO4
1	Introduction to Magnetic Contactor & Different Actuators	CLO4
1	Introduction to House hold Wiring for Single Pole one way and two way switches Scheme including UPS wiring schemes as well	CLO4
1	Project based on different Dot Matrix or Bar Display or Seven Segment or CFL PCB or Actuators on a Double sided PCB	CLO4

* - Tentative

For all Dot Matrix or Seven segment displays, display driver pre-programmed will be given to students to check their circuits

INSTRUCTORS: MR. ARSALAN A. RAHIM & MR. MUHAMMAD IJAZ SESSION: 2017 SUBJECT: ELECTRICAL AND ELECTRONICS WORKSHOP LAB

LAB PERFORMANCE EVALUATION RUBRIC (For Individual Student in a Group)

PERFORMANCE	**10-9 Excellent**	**8-7 Good**	**6-5 Satisfactory**	**4-0 Needs Improvement**
Participation of each Group Member	Used time well in lab and focused attention on the experiment. Routinely provides useful ideas when participating in the group and in classroom discussion. A definite leader who contributes a lot of effort.	Used time pretty well. Stayed focused on the experiment most of the time. Usually provides useful ideas when participating in the group and in classroom discussion. A strong group member who tries hard.	Did the lab but did not appear very interested. Sometimes provides useful ideas to group when participating in the group and in lab. A satisfactory group member who does what is required.	Participation was minimal OR student was hostile about participating. Rarely provides useful ideas when participating in the group and in classroom discussion. May refuse to participate.
Connections (Jumper wires or Vias) or Design of Circuit	Actively looks for and suggests solutions to problems. (individual) Pertaining to Design of circuit or connections of Circuits i.e. Jumper wires or vias	Refines solutions suggested by others. (individual) Complete and error free connections done. No neatness in the circuit and/or difficult to comprehend for the instructor. (Group)	Does not suggest or refine solutions, but is willing to try out solutions suggested by others. (individual) Few mistakes in connections. But neatly done, easy to comprehend for the instructor. (Group)	Does not try to solve problems or help others solve problems. Lets others do the work. (individual) Many mistakes in connections, no neatness in the circuit and/or difficult to comprehend for the instructor. (Group)
Running the Circuit Patched	Student is well prepared with the theoretical knowledge related to the experiment. (individual) Experiment is run step by step and flawlessly according to the procedure provided on the lab manual. Correct reading set. (Group)	Student is averagely prepared with the theoretical knowledge related to the experiment. (Individual) Experiment is run step by step and flawlessly according to the procedure provided on the lab manual. Correct Reading set. (Group)	Below average theoretical knowledge. (Individual) Not following the instructions mentioned on lab manual, but still manages to run the experiment anyway and/or semi correct readings set. (Group)	Poor level of theoretical knowledge. (Individual) Not able to run the experiment and/or incorrect readings. (Group)
Safety Procedures & Tool Usage	Lab is carried out with full attention to relevant safety procedures & directions. Specifically for the	Lab is generally carried out with attention to relevant safety procedures & directions.	Lab is carried out with some attention to relevant safety procedures & directions.	Safety procedures were ignored and/or some aspect of the experiment posed a threat to the safety of the student or others. Did Not follow directions.
Discipline and Behavior Workstation Ethics	Stayed in seat and got up for a specific lab-related reason. Took care of lab-related business and sat down right away. Discussed only lab related stuff with the group members. Not talking with other groups' students at tall. Voice level kept appropriate. Not used cell phones or involved in any non-lab related activity. Outstanding job cleaning up working area, and equipment. Returned all materials appropriately and responsibly.	Stayed in seat and got up for a specific lab-related reason, but took more time than required to do the job. No more than one incident of talking non-lab related stuff in lab and/or any talk with other groups, voice level exceeding the appropriate level, use of cell phones and involvement in any non-lab related activity. Good job on cleaning up working area and equipment. Returned all materials appropriately.	Got out of seat and wander around for some time. No more than two incidents of talking non-lab related stuff in lab and/or any talk with other groups, voice level exceeding the appropriate level, use of cell phones and involvement in any non-lab related activity. Had to be reminded to clean up area and equipment; and to return materials.	Got out of and wander around. Chased others, ran, or played around. More than two incidents of talking non-lab related stuff in lab and/or any talk with other groups, voice level exceeding the appropriate level, use of cell phones and involvement in any non-lab related activity. (Student might be expelled from lab for more than one weeks because of poor behavior) Had to be asked by teacher to clean up and return materials. Did not clean up area or return materials. Refused to clean up.
TOTAL	<------Total points earned (Max 50) = **Lab Performance Grade**----->			

INSTRUCTORS: MR. ARSALAN A. RAHIM & MR. MUHAMMAD IJAZ **SESSION: 2017** **SUBJECT: ELECTRICAL AND ELECTRONICS WORKSHOP LAB**

PROJECT PERFORMANCE EVALUATION RUBRIC (For Evaluation in a Group)

PERFORMANCE	**10-9 Excellent**	**8-7 Good**	**6-5 Satisfactory**	**4-0 Needs Improvement**
Space Usage and Placement of Components	Usage of space is done excellently with components placed neatly and the overall look of the circuit is neat.	Usage of space is done good with components placed almost neatly and the overall look of the circuit is OK	Usage of space is below par with components placed wide apart and the overall look of the circuit is satisfactory	Usage of space is done badly with components placed far apart with no symmetry.
Design of Circuit or PCB	Design of circuit on Vero board and PCB is neatly done with all design rules followed in PCB design pertaining to vias and orthogonal design.	Design of circuit on Vero board and PCB is neatly done with some design rules followed in PCB design pertaining to vias and orthogonal design.	Design of circuit on Vero board and PCB is neatly done with all design rules followed in PCB design pertaining to vias and orthogonal design.	Design of circuit on Vero board and PCB is neatly done with all design rules followed in PCB design pertaining to vias and orthogonal design.
Soldering Quality	Soldering Quality is excellent with no cold joints and less and efficient usage of material with no joints loose.	Soldering Quality is good with some cold joints and large usage of material with some joints loose.	Soldering Quality is satisfactory with 50% cold joints and more usage of material with many joints loose.	Soldering Quality is very poor with wires hanging if circuit is checked.
Running the Patched Circuit	Circuit ran flawlessly on first run without any trouble from the driver circuitry	Circuit ran flawlessly on second or third run with some changes in circuit at run time	Circuit ran after debugging from the teacher in charge and had problems pertaining to loose connections of faulty circuits	Circuit did not ran as required due to wrong connections and faulty design
Report with CAD Diagrams	Report contains diagrams illustrating circuit diagrams, Top Layer or Bottom Layer PCB Design with descriptions of each diagram. Also Problems Faced are asked in report for each Project.	Report contains diagrams but with less illustrations and not neatly placed.	Report contains less diagrams as required in the report with neatness and overall report quality compromised	Report not submitted
TOTAL	<------Total points earned (Max 50) = **Lab Performance Grade**----->			